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For: QUANTUM WELL INTERMIXING

Group No.:

Examiner:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Attached please find the certified copy of the foreign application from which priority is claimed for this case:

Country	**: Singapore**
Application Number	**: 200004786-0**
Filing Date	**: 11 September 2000**

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This is to certify that the annexed is a true copy of the following Singapore patent application as filed in this Registry.

Date of Filing	:	11 SEPTEMBER 2000
Application Number	:	200004786-0
Applicant(s)	:	NANYANG TECHNOLOGICAL UNIVERSITY
Title of Invention	:	SUPERLUMINESCENT DIODES

CHIG KAM TACK
Assistant Registrar
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SINGAPORE

PATENTS FORM 1 Rule 19

SINGAPORE
THE PATENTS ACT
(CHAPTER 221)
THE PATENTS RULES

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11 SEP 2000

The Registrar of Patents,
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REQUEST FOR THE GRANT OF A PATENT

THE GRANT OF A PATENT IS REQUESTED BY THE UNDERSIGNED ON THE BASIS OF THE PRESENT APPLICATION.

I. Title of Invention		**SUPERLUMINESCENT DIODES**
II. Applicant(s) (see note 2)	*(a) Name*	**NANYANG TECHNOLOGICAL UNIVERSITY**
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	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	
	(c) Name	-
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	

200004786-0

III. Declaration of Priority (see note 3)	Country/ Country Designated		*File no.*	
	Filing Date			
	Country/ Country Designated		*File no.*	
	Filing Date			
	Country/ Country Designated		*File no.*	
	Filing Date			

IV. Inventors (see note 4)				
(a) The applicant(s) is/are the sole/joint inventor(s)	[ ] *Yes*	[X] *No*		
(b) A statement on Patents Form 8 is/will be furnished.	[X] *Yes*	[ ] *No*		
V. Name of Agent (if any) (see note 5)	**HAQ & NAMAZIE PARTNERSHIP**			
VI. Address for Service (see note 6)	*Block/Hse No.*		*Level No.*	
	~~Unit No~~/PO Box	**765**	*Postal Code*	**901515**
	Street Name	**Robinson Road Post Office**		
	Building Name			
VII. Claiming an earlier filing date under section 20(3),26(6) or 47(4). (see note 7)	*Application No.*			
	Filing Date			

[Please tick in the relevant space provided]:

( ) Proceeding under rule 27(1)(a).

Date on which the earlier application was amended = _____

Or

( ) Proceeding under rule 27(1)(b)

VIII. Invention has been displayed at an International Exhibition (see note 8)	☐ *Yes* ☒ *No*
IX. Section 114 requirement (see note 9)	*The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depositary authority under the Budapest Treaty.* ☐ *Yes* ☒ *No*
X. Check List (To be filled in by applicant or agent)	A. The application contains the following number of sheet(s):-

1. Request	**4**	*sheets*
2. Description	**22**	*sheets*
3. Claim(s).	**6**	*sheets*
4. Drawing(s).	**5**	*sheets*
5. Abstract.	**1**	*sheets*

B. The application as filed is accompanied by:-

1. Priority document	
2. Translation of priority document	
3. Statement of Inventorship & right to grant	X
4. International Exhibition Certificate	

XI. Signature(s) (see note 10)	*Applicant (a)*	
	Date	**11 SEPT. 2000**
	Applicant (b)	
	Date	
	Applicant (c)	
	Date	

NOTES :

1. This form when completed, should be brought or sent to the Registry of Patents together with the prescribed fee and 3 copies of the description of the invention, and of any drawings.

2. Enter the name and address of each applicant in the spaces provided at paragraph II. Names of individuals should be indicated in full and the surname or family name should be underlined. The names of all partners in a firm must be given in full. The place of residence of each individual should also be furnished in the space provided. Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that should be entered where provided. Where more than three applicants are to be named, the names and address of the fourth and any further applicants should be given on a separate sheet attached to this Form together with the signature of each of these further applicants.

3. The declaration of priority at paragraph III should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under the Patents (Convention Countries) Order] should be identified and the name of that country should be entered in the space provided.

4. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph IV should be completed by marking the 'YES' Box in the declaration (a) and the 'NO" Box in the alternative statement (b). Where this is not the case, the 'NO' Box in declaration (a) should be marked and a statement will be required to be filed on Patents Form 8.

5. If the applicant has appointed an agent to act on his behalf, the agent's name should be indicated in the spaces available at paragraph V.

6. An address for service in Singapore to which all documents may be sent must be stated at paragraph VI. It is recommended that a telephone number be provided if an agent is not appointed.

7. When an application is made be virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified at paragraph VII and the number of the earlier application or any patent granted thereon identified.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)©, then the 'YES' box at paragraph VIII should be marked. Otherwise the 'NO' box should be marked.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' box at paragraph IX should be marked. Otherwise the 'NO' box should be marked.

10. Attention is drawn to rules 90 and 105 of the Patent Rules. Where there are more than three applicants, see also Note 2 above.

11. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least two months after the application has been filed in Singapore.

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SUPERLUMINESCENT DIODES

Field of the invention

The present invention relates generally to the field of superluminescent diodes, and more particularly to a method of manufacture of such diodes. It also relates to superluminescent diode structures.

Background of the invention

Superluminescent diodes (SLDs) are light emitting devices in which stimulated emission takes places, but without sufficient gain being present to cause lasing action to occur. SLDs have characteristics of high output power and low beam divergence, which are similar to the characteristic of an injection laser diode (LD). SLDs also give a broad emission spectrum and low coherence length, which are similar to a light emitting diode (LED). Whereas laser diodes produce fully coherent optical output, SLDs do not, instead producing output line widths of typically 15-20 nm. Increase in line width is desirable in many applications, and line width greater than 60 nm has been achieved with our design.

Superluminescent diodes are not only applied to short and medium distance communication systems, but also are key elements in the interferometric fiber-optic gyroscope (IFOG) system and other fiber-optic based sensing systems. A further application of such diodes is testing or diagnosis using optical coherence tomography. SLDs allow the elimination of modal noise in fiber systems, and provide immunity to optical feedback noise and high coupling efficiency into fibers. The broadband characteristics of SLDs provide low Rayleigh backscattering noise, low polarization noise and low bias offset due to the non-linear Kerr effect in fiber gyro systems.

The coherence length of a light source is a property indicative of the phase-purity of the light source with respect to the wavelength of the light emitted. Viewed from one perspective, the coherence length is descriptive of the difference in path length between an original beam and a secondary beam; it is thus analogous to photographic depth of focus. The coherence length may be defined as the propagation distance from a source to a point where the wave from the source maintains a specific coherence. It is typically approximated by the square of the mean wavelength of the

source divided by (refractive index times spectral width). Thus, as the spectral width broadens, the coherence length is reduced.

In order to produce a broad spectrum SLD from the quantum well materials, it has previously been proposed to use stacked quantum wells having two active layers which have a bandgap difference of 70 nm. This however requires a complex manufacturing process. Additionally the diodes fabricated in this way tend to have a relatively narrow linewidth and limited power.

It is accordingly an object of the present invention to provide a simplified and/or improved method of making a superluminescent diode.

It is a further object of the present invention to provide a method of making superluminescent diodes which have improved properties with respect to prior art diodes.

It is yet a further object of the present invention to provide a superluminescent diode at least some of whose properties are improved with respect to prior art diodes.

Summary of the invention

According to a first aspect of the present invention there is provided a method of making a superluminescent diode comprising providing a semiconductor structure comprising a quantum well region, implanting impurities into a surface of said structure such that the density of said impurities has a spatial variation over said quantum well region, and annealing said structure.

Preferably said implanting step comprises providing a surface layer on said structure, etching away portions of said surface layer over said quantum well region to provide a spatially varying thickness of said surface layer over said quantum well region and implanting said impurities through said surface layer.

In one embodiment said etching step comprises providing a masking layer having a pattern with a mask zone of predetermined width, the masking layer having a first higher density and substantially a step change to a second lower density at a first edge of said mask zone and a density which

rises across said width from said second lower density to substantially said first higher density.

Preferably. said density varies substantially linearly across said width.

In a second embodiment, said etching step comprises providing a masking layer having a predetermined width, said width containing first and second opposing distal regions and an intermediate region, said first distal region containing a transition from a first higher mask density to a second lower density, said second distal region containing a transition from substantially the second lower density to substantially the first higher density, and said intermediate region being at substantially said second lower density.

Preferably said intermediate region has constant density.

Preferably said etching step comprises performing a dry etching process.

Conveniently said dry etching process comprises reactive ion etching.

Advantageously said surface layer comprises a dielectric, or a metal.

Conveniently said surface layer comprises silicon dioxide.

According to a second aspect of the invention there is provided a method of manufacturing a superluminescent diode comprising providing a surface layer on a surface of a semiconductor structure comprising a quantum well region, wherein said surface layer has a spatially varying thickness over said quantum well region and performing quantum well intermixing on said structure by impurity-induced disordering, hereinafter referred to as "IID", wherein during the implantation step of said quantum well structure, said impurities are implanted through said surface layer.

In one embodiment said step of providing a surface layer comprises forming a substantially uniform thickness layer over said quantum well region, providing a masking layer including a gray mask, said gray mask having a predetermined width, having a first higher density and substantially a step change to a second lower density at a first edge thereof and a

varying density which rises across said width from said second lower density to substantially said first higher density, and etching said uniform thickness layer.

Preferably said density varies substantially linearly across said width.

Preferably said etching step comprises performing a dry etching process.

Conveniently said dry etching process comprises reactive ion etching.

Advantageously said surface layer comprises a dielectric, or a metal.

Conveniently said surface layer comprises silicon dioxide.

In a second embodiment, said step of providing a surface layer comprises forming a layer of substantially uniform thickness over said quantum well region, providing a masking layer having a predetermined width, said width containing first and second opposing distal regions and an intermediate region,

said first distal region containing a transition from a first higher mask density to a second lower density, said second distal region containing a transition from substantially the second lower density to substantially the first higher density, and said intermediate region being at substantially said second lower density.

Preferably said intermediate region has constant density.

Preferably said etching step comprises performing a dry etching process.

Conveniently said dry etching process comprises reactive ion etching.

Advantageously said surface layer comprises a dielectric, or a metal.

Conveniently said surface layer comprises silicon dioxide.

In one embodiment said impurities comprise As ions.

In a second embodiment said impurities comprise P ions.

Another aspect of the present invention provides a device for providing high output power with short coherence length and wide spectral bandwidth comprising an active region and an absorption region. In this aspect of the invention, the active region comprises a spatially-varying quantum well intermixing profile thus providing a broad emission spectrum with high gain while the absorption region provides the means for suppressing laser operation.

The cross section of the spatially-varying quantum well intermixing profile in the active region can be of any form. For example the cross-section can be trapezoidal, triangular or Gaussian in shape.

The ratio of the active and absorption region is variable providing many embodiments of the device.

In other embodiments of the device of the present invention, the material of the device is selected from a group comprising Gallium, Arsenic, Phosphorus and Indium.

The pattern of the active and absorption region may be variable providing various embodiments of the device. For example, the pattern may be straight and perpendicular to the output facet. The pattern may also be a curve or slanted at an angle to the output facet. The pattern may further be funnel-shaped with the wider end being located at the output facet.

In another embodiment of the present invention, the device has a coating at the output facet to provide anti-reflection.

According to another aspect of the invention there is provided a superluminescent diode comprising a semiconductor structure having a quantum well region, said quantum well region being intermixed by impurity induced disordering implanting, wherein said impurities have a density which varies with respect to distance across the quantum well region.

The present invention also provides a device which saves cost on expensive multi-layer anti-reflection coating.

Brief description of the drawings

Figure 1 shows a diagram of a structure from which SLDs were developed;

Figure 2 shows an exemplary process flow in accordance with the invention for producing SLDs;

Figure 3 shows a schematic diagram of a fabricated discrete SLD;

Figure 4 is a diagram showing the spectra of the active section of the As^{++} and P^{++} -IID SLDs;

Figure 5 is a diagram showing the intensity versus applied current curves of the active section of the As^{++} and P^{++} -IID SLDs;

Figure 6 shows the normalized spectral emission from the four types of SLDs under the same pumping conditions

Figure 7 shows the non-normalized spectral emission of the As^{++} SLDs with mutually different pumping currents; and

Figure 8 shows the non-normalized spectral emission of the P^{++} -IID SLDs with mutually different pumping currents.

Description of the preferred embodiments

To obtain high output power from an SLD, a very high optical gain is necessary within the device, consequently suppression

of lasing is a key concern. The suppression techniques can be divided into two categories. The first category comprises active suppression methods such as using an un-pumped absorber, short-circuited absorber and bending-waveguide approaches. The second category comprises passive suppression methods such as using a non-absorbing window, angled-stripe and antireflection coating (AR) approaches. The scheme of combining the active region with an un-pumped absorbing region was selected here as this structure has been successfully demonstrated to produce high performance SLDs. Using this suppression method, it is believed that with the un-pumped absorber (neither metal contact nor current injection) and as-grown bandgap, the light emitted from the active region (wider bandgap)[6,7] can be fully absorbed and laser oscillation can be effectively suppressed.

Referring to figure 1, an SLD chip was formed using an InP/InGaAs/InGaAsP structure (1) grown using metal organic chemical vapour deposition (MOCVD) on an InP substrate (10). An active region (11) was undoped and consisted of a 5.5 nm wide InGaAs quantum well (20), with a pair of 12 nm InGaAsP (λ_g=1.26 μm) barriers (21,22) one disposed on each side of the

quantum well, where λ_g is the bandgap wavelength. The active region was bounded on each side by pairs of graded index (GRIN) confining layers of InGaAsP (23,24;25,26). The thickness and composition of these layers were 50 nm of λ_g=1.18 μm (23,25) and 80 nm of λ_g=1.05 μm (24,26), respectively. The structure was lattice matched to InP throughout, and was completed with a 1400 nm InP upper cladding layer (30), and a contact layer formed from a supervening layer of 65 nm thickness InGaAsP followed by a 10 nm thickness InGaAs top layer (32). The lower cladding layer (12) was sulfur-doped to a concentration of 2.5×10^{18} cm^{-3}. The upper cladding layer (30) was doped with Zn to a concentration of 7.4×10^{17} cm^{-3}, and the supervening layer and top layer were doped with 2×10^{18} cm^{-3} and 1.3×10^{19} cm^{-3} concentration of Zn, respectively. The core of the structure was undoped, thus forming a P-I-N structure with the intrinsic region restricted to the quantum well and GRIN layers.

The present invention makes use of a technique for controlling the bandgap of the quantum well semiconductor structure by quantum well intermixing and uses a process known as impurity-induced disordering(IID). This process has a first stage in

which impurities are implanted into the quantum well material. In a later stage the structure is annealed to thereby induce diffusion of both impurity and point defects into the quantum wells and barriers, and hence interdiffusion of matrix elements between quantum wells and barriers. In the InGaAs/InGaAsP quantum well device of the embodiment, interdiffusion of Group V elements from barrier to well results in blue shifting the bandgap energy. The effects are believed mainly to be caused by three mechanisms, namely diffusion of point defects generated during the implantation process, self-interdiffusion at elevated temperature (thermal shift) and diffusion of the implanted species.

The bandgap of the quantum well region in the SLD chip was spatially varied by causing the implantation of impurities to vary. This was achieved in different embodiments by implanting through profiled mask stripes, the profiles being referred to herein as "triangular" and "trapezoidal" patterns. Hereinafter a "triangular-pattern" signifies that mask transmissivity varies across the width of the mask stripe slopewise from maximum thickness (minimum transmission) to minimum thickness (maximum transmission). In the embodiment described, the thickness tapers linearly with distance, but non-linear

variations are also possible. Hereinafter, a "trapezoidal-pattern" signifies that mask transmissivity varies across the mask stripe from maximum thickness (minimum transmission) to minimum thickness (maximum transmission) and back to maximum thickness. In the embodiment described, the "trapezoidal-pattern" has generally symmetrical opposing edge regions of relatively sharp linear fall in thickness and a central region of constant thickness, which central region provides maximum transmission. It will however be clear that symmetry is not always necessary and that the central region may exhibit thickness variation.

It is also clear that although the described embodiments have a minimum thickness of zero - i.e. 100% transparent - it is also possible to perform the invention with a non-zero minimum thickness.

For the present embodiments, the stripe width was selected to be the same for both types of pattern.

Two chips were used for the fabrication of SLDs. A first was intended to be implanted using an As^{++} IID process and a second using a P^{++} IID process. A simulation process was used to

determine what thickness of mask material would totally block the penetration of As and P ions during implantation. In this case, SiO_2 was selected as mask material, but it will be clear to those skilled in the art that other materials could be substituted, including other dielectrics or metals. The thickness of SiO_2, corresponding to the above discussed "maximum thickness" of mask, was approximately 400-700 nm for As and 600-1000 nm for P respectively.

Three mask levels were used in an exemplary process for fabricating SLDs. The first mask level provides for the definition of alignment marks. Referring to figure 2, the second mask level is the gray mask, used in a first embodiment to create diodes having triangular pattern masks and in a second embodiment to create diodes having trapezoidal pattern masks. The third mask level defines the active contact window and the absorber section. As shown in figure 3, the active section (40) has a stripe pattern (41). Each stripe has a typical width 50 ~ 100 μm.

The alignment marks were first defined by wet etching down to the InPupper cladding layer (30). After the etching process,

the first and second chips were coated with SiO_2 of suitable thickness to obtrude the impurity doping for which they were destined. As noted above the first chip (destined for As^{++}) was coated with around 400-700 nm of SiO_2 and the second chip (destined for implantation of P^{++}) was coated with around 600-1000 nm of SiO_2.

Next a photo-resist (or "resist" in short) was applied and the masking step was carried out, followed by mask development in the case of the first embodiment producing the triangular pattern of mask and in the second, producing the trapezoidal pattern of mask.

After obtaining the desired resist pattern, dry etching for example reactive ion etching - was then carried out to transfer the resist pattern into a mask, in this embodiment SiO_2. After preparing the graded SiO_2 patterns, the first chip was then implanted with As impurities at 150°C ~ 230°C with a dose of $1x10^{12}$ to $1x10^{14}$ cm^{-2}, and the second chip was implanted with P impurities under similar conditions.

It will be appreciated that other mask materials could be used, for example silicon nitride, instead of SiO_2.

Quantum well intermixing was then carried out by rapid thermal processing at 500°C ~ 800°C for about 80s ~ 120s, retaining the SiO_2 implant mask. After this, the SiO_2 mask was removed completely, e.g. by etching.

Some exemplary process parameters for the process are listed in Table 1.

Table 1. Exemplary process parameters for the fabrication of As^{++} and P^{++} SLDs.

SLD	***SiO_2 thickness (μm)***	***Photoresist (thickness, spin speed, spin time)***	***UV exposure time (s)***
As^{++}	0.4-0.7	0.6-0.9 μm, 4000-6000 rpm, 30-60 s	2-8
P^{++}	0.6-1.0	0.8-1.2 μm, 4000-6000 rpm, 30-60 s	2-8

The SLD chips were then cleaved into diodes having a 1300 μm length of active section and 950 μm of absorbing section for intensity versus applied current measurements at high current injection. An exemplary SLD fabricated using this invention is shown in figure 3. Referring to figure 3, it will be seen

that, as previously mentioned, the active section has a stripe for a metal surface contact, whereas the absorbing section which was not implanted, and thus not intermixed, but which was annealed - had no conductive contact. A 500 μm length of active section was also cleaved out from the intermixed SLD section of each type of SLD to assess luminescence emission spectra, and the intensity versus applied current characteristic.

Referring now to figure 4, in general the SLDs of the second profile embodiment i.e. trapezoidal profiled - from both As^{++} and P^{++} doped IID chips, can be seen to have received a slightly higher degree of quantum well intermixing than the triangular-profiled SLDs of the first profile embodiment. The difference is seen to be about 4 to 8 nm.

With reference to figure 5, the triangular-profiled SLDs of the first embodiment have a similar or better threshold current to the as-grown lasers. However, the threshold current density for trapezoidal-profiled SLDs increased slightly but still was roughly 20 % higher than that of the as-grown laser. The higher degree of intermixing and slight degradation of

quality observed from the trapezoidal-profiled SLDs may be attributed to having a larger area receiving direct implantation than the triangular-profiled SLDs.

Referring to figure 6, the normalized emission spectra were determined using the same pumping current, here 2.5 A. In general, triangular-profiled SLDs have a wider spectrum than the trapezoidal-profiled SLDs. A FWHM of up to 60 nm, the broadest spectrum, was obtained from the As^{++}-IID triangular-profiled SLDs. This embodiment also has the shortest coherence length of 35 μm. A summary of the results is shown in Table 2. Due to limitations of the measurement set-up, the spectral modulation depth of each SLD was not determined.

Figures 7 and 8 show the non-normalized emission spectra of the As^{++} and P^{++} doped IID SLDs with different pumping currents. Here, Figure 7(a) and Figure 8(a) refer to the triangular-profiled SLDs while Figure 7(b) and Figure 8(b) refer to the trapezoidal-profiled SLDs. It was found that As^{++} doped IID SLDs started to have lasing mode with injection current above 2.8 A. In order to suppress the lasing mode, some methods, such as coating an antireflection (AR) layer on the front

facet or short-circuiting of the absorber section or both, can be done. If this is done, higher current injection and higher output power can be obtained without triggering the lasing mode of the diode.

Table 2. Summary of measurement results for the As^{++} and P^{++} IID processed SLDs.

Type of SLDs	***Center Wavelength, λ(nm)***	***FWHM, Δλ(nm)***	***Coherence length, $\lambda^2/\Delta\lambda$ (μm)***
As^{++} triangular	1454	60	35.24
As^{++} trapezoidal	1444	44.8	46.54
P^{++} triangular	1460	51.7	41.23
P^{++} trapezoidal	1449	43.5	48.27

It is observed that the SLD with the broadest spectrum, as large as 60 nm, was obtained from the As^{++} doped IID triangular-profiled sample. The spectrum is expected to be able to further expand by optimizing the graded profile of the SiO_2 implant mask to achieve a higher degree of and more uniform quantum well intermixing across the implant mask.

It is also understood by those skilled in the art that routine practices including the following can be applied to enhance the performance and functionality of the said superluminescent diodes:-

1) The diode consists essentially of two portions: an active region with current pumping and an un-pumped absorber region. Measurements have been done with active regions of length 1300 μm and absorbing sections of 950 μm length. Here, variations in the active region length to absorbing section length ratio are possible for higher output powers.

2) Higher output reliability and efficiency can be achieved by incorporating a non-absorbing output facet through the same quantum well intermixing process to minimize degradation at the output facet.

3) The devices described in this invention has a uniform stripe design. However, stripes with varying widths, like a broadening one towards the output facet, can be introduced to control the mode profile.

4) In this invention, the impurity implantation is implemented using triangular and trapezoidal oxide mask profiles. Other oxide mask profiles of Gaussian, exponential or any arbitrary shape could also be adopted.

5) Although superluminescent diode emitting at around 1.5 μm have been demonstrated, the process technology and device structure can also be applied to devices operating at other wavelengths.

Claims

1. A method of making a superluminescent diode comprising providing a semiconductor structure comprising a quantum well region, implanting impurities into a surface of said structure such that the density of said impurities has a spatial variation over said quantum well region, and annealing said structure.

2. The method of claim 1 wherein said implanting step comprises providing a surface layer on said structure, etching away portions of said surface layer over said quantum well region to provide a spatially varying thickness of said surface layer over said quantum well region and implanting said impurities through said surface layer.

3. The method of claim 2, wherein said etching step comprises providing a masking layer having a pattern with a mask zone of predetermined width, the masking layer having a first higher density and substantially a step change to a second lower density at a first edge of said mask zone and a density which rises across said width from said second lower density to substantially said first higher density.

4. The method of claim 3, wherein said density varies substantially linearly across said width.

5. The method of claim 2, wherein said etching step comprises providing a masking layer having a predetermined width, said width containing first and second opposing distal regions and an intermediate region, said first distal region containing a transition from a first higher mask density to a second lower density, said second distal region containing a transition from substantially the second lower density to substantially the first higher thickness, and said intermediate region being at substantially said second lower density.

6. The method of claim 5 wherein said intermediate region has constant density.

7. A method of making a superluminescent diode comprising providing a semiconductor structure comprising a quantum well region, providing a surface layer on said structure, etching away portions of said surface layer over said quantum well region to provide a spatially varying thickness of said surface layer over said quantum well region and implanting said impurities through said surface layer into a surface of said structure such that the density of said impurities has a spatial variation over said quantum well region, and annealing said structure wherein said etching step comprises performing a dry etching process.

8. The method of claim 7 wherein said dry etching process comprises reactive ion etching.

9. The method of claim 7 or 8 wherein said surface layer comprises a dielectric, or a metal.

10. The method of claim 7 or 8 wherein said surface layer comprises silicon dioxide.

11. A method of manufacturing a superluminescent diode comprising providing a surface layer on a surface of a semiconductor structure comprising a quantum well region, wherein said surface layer has a spatially varying thickness over said quantum well region and performing quantum well intermixing on said structure by impurity-induced disordering, wherein during the implantation step of said quantum well intermixing, said impurities are implanted through said surface layer.

12. The method of claim 11 wherein said step of providing a surface layer comprises forming a substantially uniform thickness layer over said quantum well region, providing a masking layer including a gray mask, said gray mask having a predetermined width, having a first higher density and substantially a step change to a second lower density at a first edge thereof and a varying density which rises across said width from said second lower density to substantially

said first higher density, and etching said uniform thickness layer.

13. The method of claim 12 wherein said density varies substantially linearly across said width.

14. The method of claim 12 wherein said etching step comprises performing a dry etching process.

15. The method of claim 11 wherein said step of providing a surface layer comprises forming a layer of substantially uniform thickness over said quantum well region, providing a masking layer having a predetermined width, said width containing first and second opposing distal regions and an intermediate region, said first distal region containing a transition from a first higher mask density to a second lower density, said second distal region containing a transition from substantially the second lower density to substantially the first higher thickness, and said intermediate region being at substantially said second lower density.

16. The method of claim 15 wherein said intermediate region has constant density.

17. The method of claim 16 wherein said etching step comprises performing a dry etching process.

18. The method of claim 17 wherein said dry etching process comprises reactive ion etching.

19. The method of claim 11 wherein said surface layer comprises a dielectric, or a metal.

20. The method of claim 11 wherein said surface layer comprises silicon dioxide.

21. The method of claim 11 wherein said impurities comprise arsenic ions.

22. The method of claim 11 wherein said impurities comprise phosphorous ions.

23. A superluminescent diode comprising a semiconductor structure having a quantum well region, said quantum well region being intermixed by impurity induced disordering, wherein said impurities have a density which varies with respect to distance across the quantum well region.

24. A device for providing high output power with short coherence length and wide spectral emission bandwidth comprising an active region and an absorption region.

25. A device according to claim 24 wherein the active region comprises a spatially varying quantum well intermixing profile.

26. A device according to claim 25 wherein the active region provides a broad emission spectrum.

27. A device according to claim 24 wherein the absorption region provides suppression for laser operation.

28. A device according to claim 24 wherein the active region has a trapezoidal quantum well intermixing cross-section.

29. A device according to claim 24 wherein the active region has a triangular quantum well intermixing cross-section.

30. A device according to claim 24 wherein the active region has a Gaussian cross-section.

31. A device according to claim 24 wherein the ratio of the active and absorption region is variable.

32. A device according to claim 1 wherein the material of the device is selected from a group comprising Gallium, Arsenic, Phosphorus and Indium.

ABSTRACT OF THE DISCLOSURE

TITLE: SUPERLUMINESCENT DIODES

A method of manufacturing of superluminescent diode that consists of an active region and an absorbing region. The device consists of creating a mask with spatially varying profile across an active region of the semiconductor structure having a quantum well region, implanting impurities through the mask and then annealing to achieve quantum well intermixing. The absorbing region is not subjected to quantum well intermixing.

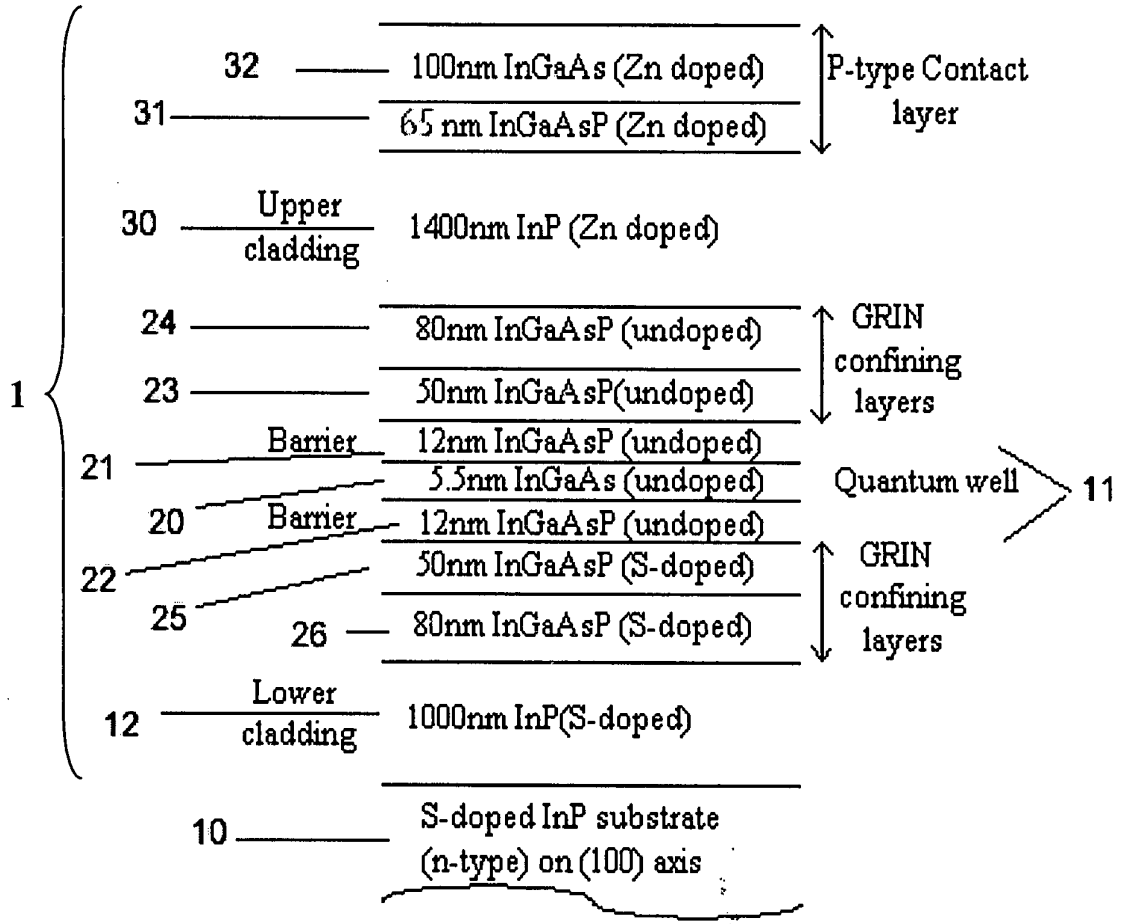
1
32
100nm InGaAs (Zn doped)
P-type Contact layer
31
65 nm InGaAsP (Zn doped)
30
Upper cladding
1400nm InP (Zn doped)
24
80nm InGaAsP (undoped)
GRIN confining layers
23
50nm InGaAsP(undoped)
21
Barrier
12nm InGaAsP (undoped)
5.5nm InGaAs (undoped)
Quantum well
11
20
Barrier
12nm InGaAsP (undoped)
22
50nm InGaAsP (S-doped)
GRIN confining layers
25
26
80nm InGaAsP (S-doped)
12
Lower cladding
1000nm InP(S-doped)
10
S-doped InP substrate (n-type) on (100) axis

Figure 1

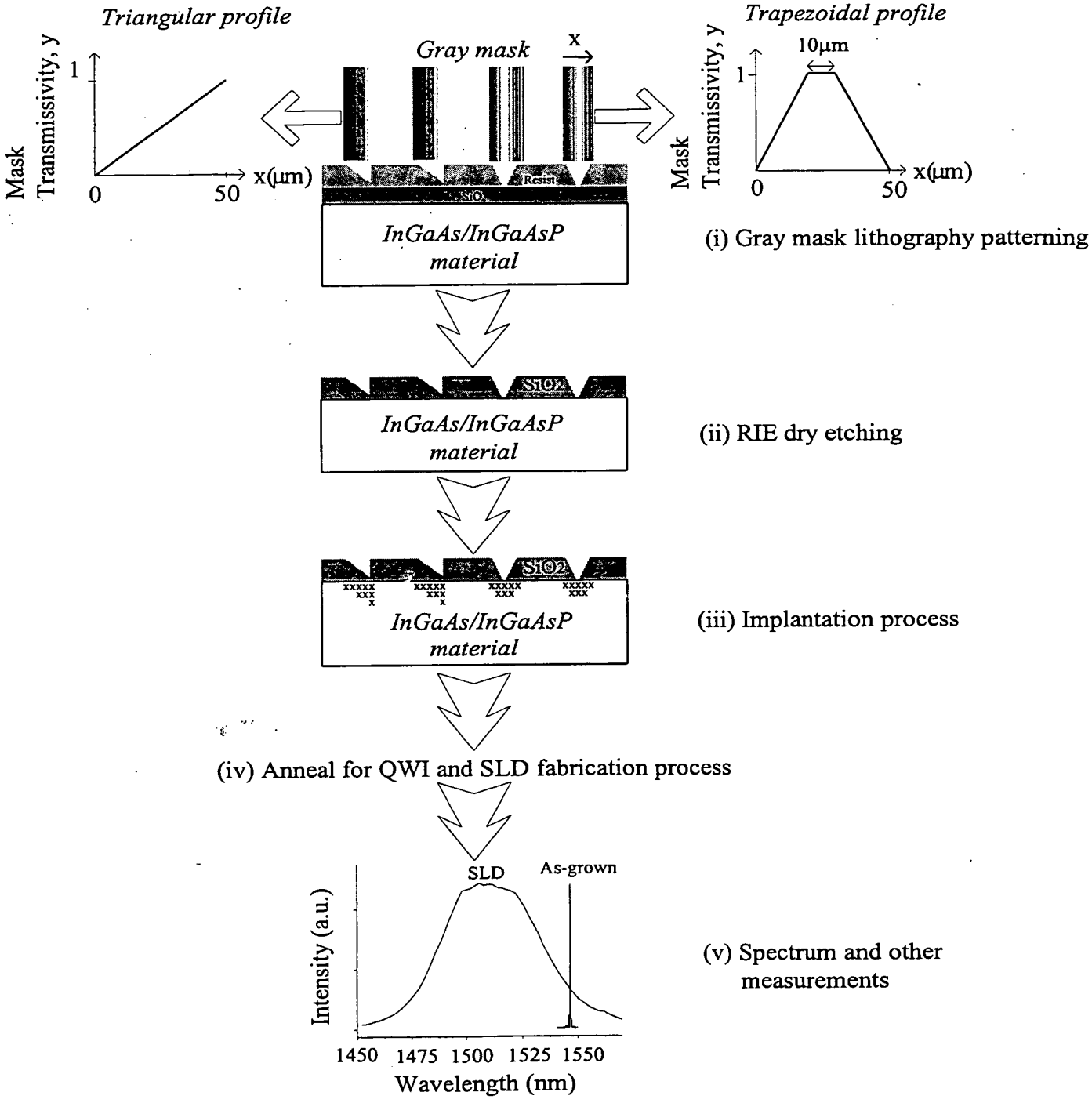
Triangular profile
Mask Transmissivity, y
1
0
50
x(μm)
Gray mask
x
Trapezoidal profile
10μm
Mask Transmissivity, y
1
0
50
x(μm)
Resist
SiO2
InGaAs/InGaAsP material
(i) Gray mask lithography patterning
SiO2
InGaAs/InGaAsP material
(ii) RIE dry etching
SiO2
InGaAs/InGaAsP material
(iii) Implantation process
(iv) Anneal for QWI and SLD fabrication process
SLD
As-grown
Intensity (a.u.)
1450 1475 1500 1525 1550
Wavelength (nm)
(v) Spectrum and other measurements

Figure 2

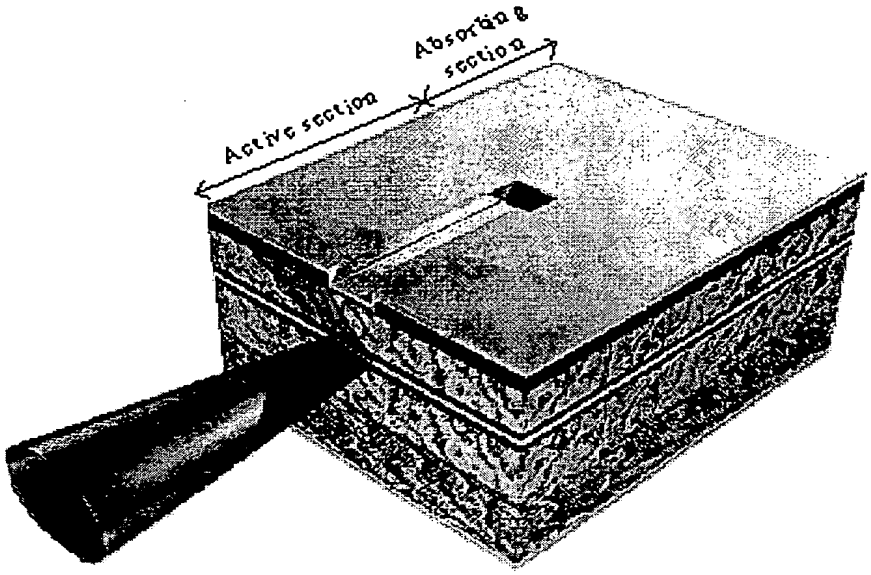

Figure 3

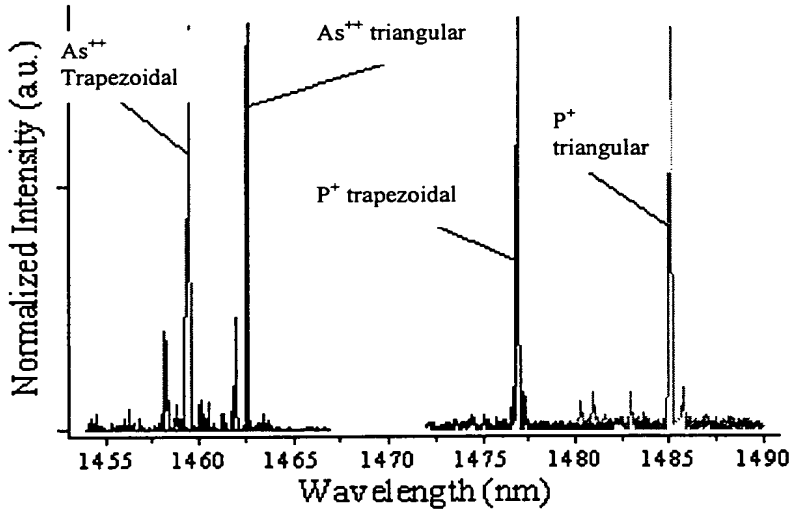

Figure 4

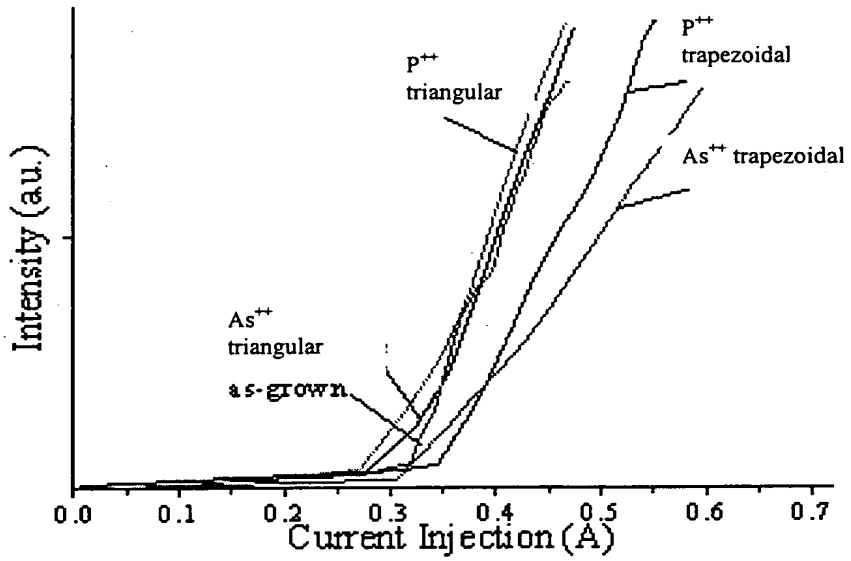

Figure 5

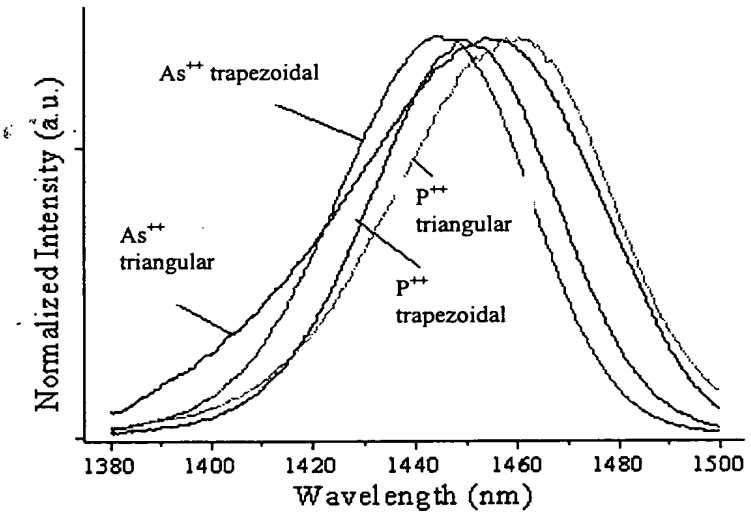

Figure 6

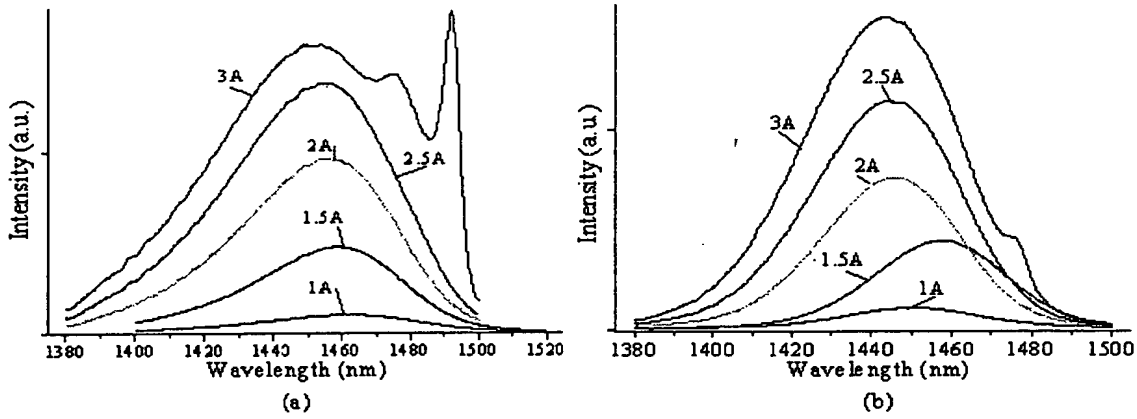

Figure 7

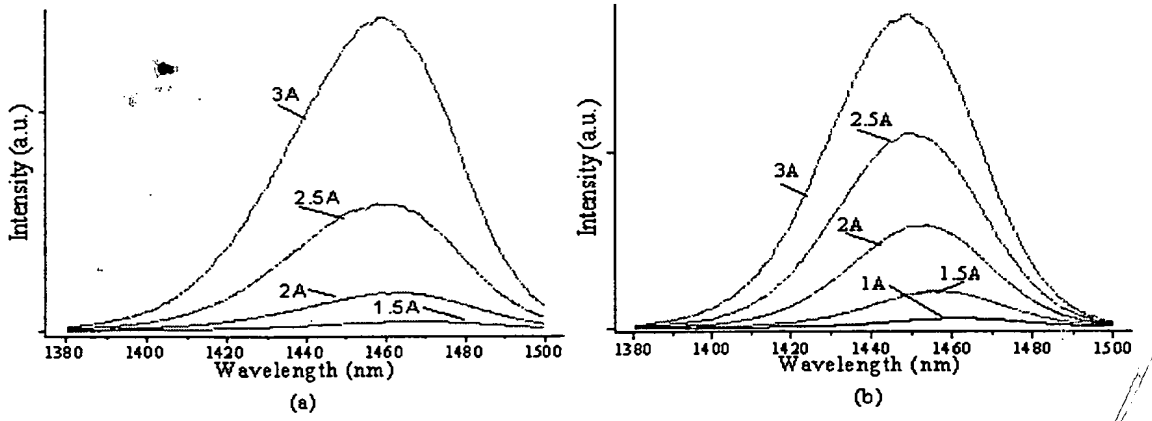

Figure 8